RAiO

RA0086A

80 CH Segment/Common Driver

For Dot Matrix LCD

Specification

Simplify Version 1.1

December 29, 2009

RAiO Technology Inc.

1. Introduction

The RA0086A is an 80 channels LCD driver LSI which is fabricated by low power CMOS high voltage process technology. It can be used either as a COMMON driver or as a SEGMENT driver, by connecting its CS input to VDD or VSS. In segment driver mode, it can be interfaced in 1-bit serial or 4-bit parallel method by the controller. In common driver mode, dual type mode is applicable. And in segment mode application, the power down function reduces power consumption.

2. Features

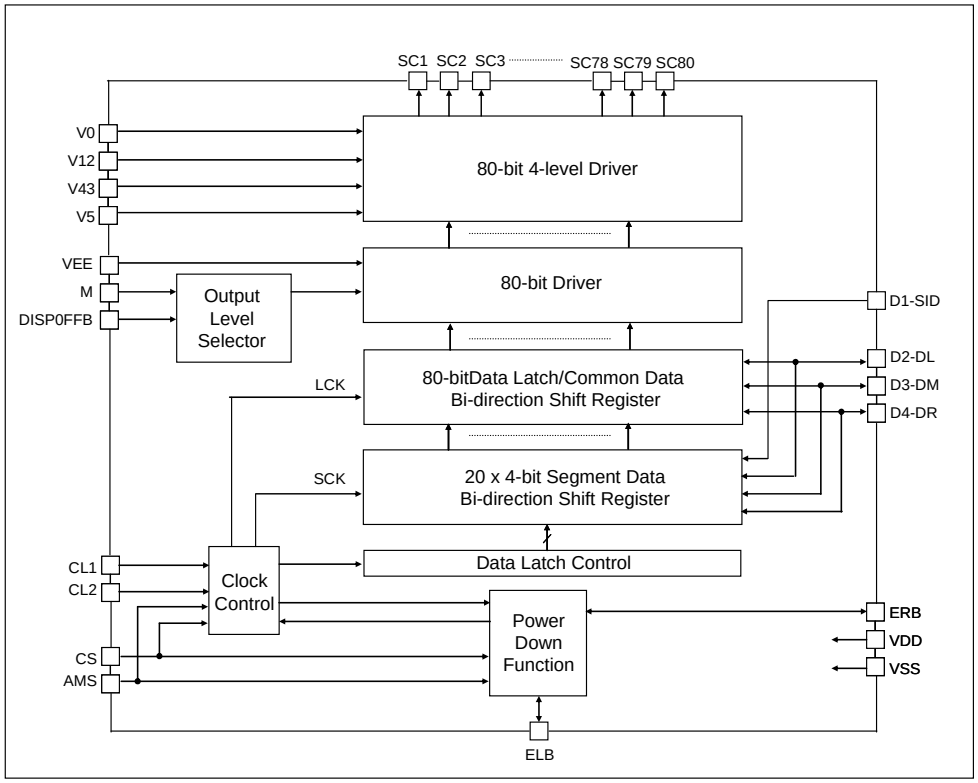
- Power supply voltage: + 5V±10 %, + 3V± 10%
- Supply voltage for display: 6 to 30V (V_{DD}-V_{EE})
- In 80-SEGMENT driver or 80-COMMON driver selection, to set CS-pin voltage is VSS or VDD
- 4-bit parallel / 1-bit serial data processing (in segment mode)
- Single mode / dual mode operation (in common mode)
- Power down function (in segment mode)
- Applicable LCD duty: 1/64 – 1/256
- Interface

Drivers	
COM(Cascade)	SEG(Cascade)
RA0086A	RA0086A

- High voltage CMOS process
- Available package Type: LQFP-100 pin, Die

Parts Number	Package
RA0086AL3N	LQFP-100 pin

3. Block Diagram



4. Signal Description

4-1 Block Description

Name	Function	COM / SEG
Clock control	Generates latch clock (LCK), shift clock (SCK) and control clock timing according to the input of CL1, CL2 and control inputs (CS, AMS). In common driver application mode, this block generates the shift clock (LCK) for the common data Bi-directional shift register.	COM / SEG
Data latch control	Determines the direction of segment data shift, and input data of each Bi-directional shift register. In 4-bit segment data parallel transfer mode, data is shifted by a 4-bit unit. In common driver application mode, data is transferred to the common data shift register directly, which disables this block.	SEG
Power down function	Controls the clock enable state of the current driver according to the input value of enable pin (ELB or ERB). If enable input value is “Low”, every clock of the current driver is enabled and the clock control block works. But if enable input is “High”, current driver is disabled and the input data value has no effect on the output level. So power consumption can be lowered.	SEG
Output level selector	Controls the output voltage level according to the input control pin (M and DISPOFFB).	COM / SEG
20x4-bit segment data BI-directional shift register	Stores output data value by shifting the input values. In 1-bit serial interface mode application, all 80 shift clocks (SCK) are needed to store all the display data. But in 4-bit parallel transfer mode application, only 20 clocks are needed. In common driver application mode, this block does not work.	SEG
80-bit data latch / common data BI-directional shift register	In segment driver application mode, the data from the 20x4-bit segment data shift register are latched for segment driver output. In single-type common driver application,1-bit input data (from DL or DR pin) is shifted and latched by the direction according to the SHL signal input. In dual-type common application mode, 80-bit registers are divided by two blocks and controlled independently.	COM / SEG
80-bit level shifter	Voltage level shifter block for high voltage part. The inputs of this block are of logical voltage level and the outputs of this block are at high voltage level value. These values are input in to the driver.	SEG
80-bit 4-level driver	Selects the output voltage level according to M and latched data value. If the data value is "High" the driver output is at selected voltage level (V0 or V5), and in the reverse case the driver output value is at the non-selected level (V12 or V43). In segment driver application mode, non-selected output value is V2 or V3. and when in common driver application, this value becomes V1 or V4.	SEG

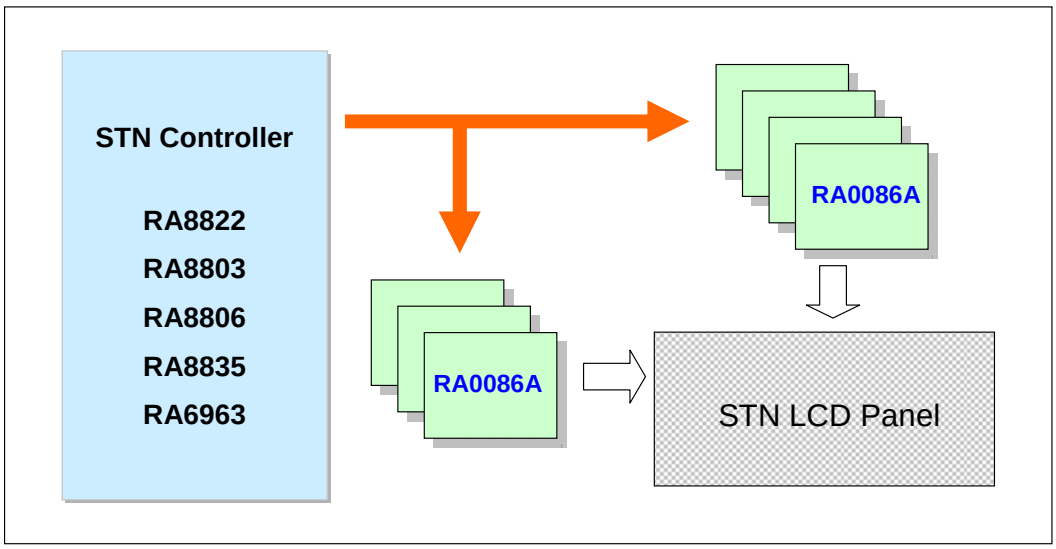
4-2 Pin Description

<table>
<tr><th>Pin</th><th>I/O</th><th>Name</th><th>Description Function</th><th>Interface</th></tr>
<tr><td>VDD</td><td rowspan="3">P</td><td rowspan="3">Power supply</td><td>Logical "High" input port (+5V ± 10%, +3V ± 10%)</td><td rowspan="3">Power</td></tr>
<tr><td>VSS</td><td>0V (GND)</td></tr>
<tr><td>VEE</td><td>Logical "Low" for high voltage part</td></tr>
<tr><td>V0, V12, V43, V5</td><td>I</td><td>LCD driver output voltage level</td><td>Bias supply voltage input to drive the LCD. Bias voltage divided by the resistance is usually used as a supply voltage source.</td><td>Power</td></tr>
<tr><td>SC1 - SC80</td><td>O</td><td>LCD driver output</td><td>Display data output pin which corresponds to the respective latch contents. One of V0, V12, V34 and V5 is selected as a display driving voltage source according to the combination of the latched data level and M signal.</td><td>LCD</td></tr>
<tr><td>CL2</td><td>I</td><td>Data shift clock</td><td>Clock pulse input for the bi-directional shift register.
– In segment driver application mode, the data is shifted to 20 x 4-bit segment data shift.
The clock pulse, which was input when the enable bit (ELB/ERB) is in not active condition, is invalid.
– In common driver application mode, the data is shifted to 80-bit common data bi-directional shift register by the CL1 clock.Hence, this clock pin is not used (Open or connect this pin to VDD).</td><td>Controller</td></tr>
<tr><td>M</td><td>I</td><td>AC signal for LCD driver output</td><td>Alternate signal input pin for LCD driving.
Normal frame inversion signal is input in to this pin.</td><td>Controller</td></tr>
<tr><td>CL1</td><td>I</td><td>Data latch clock</td><td>– In segment driver application mode, this signal is used for latching the shift register contents at the falling edge of this clock pulse. CL1 pulse "High" level initializes power-down function block.
– In common driver application mode, CL1 is used as a shifting clock of common output data.</td><td>Controller</td></tr>
<tr><td>DISPOFFB</td><td>I</td><td>Display OFF control</td><td>Control input pin to fix the driver output (SC1~SC80) to V0 level,during "Low" value input. LCD becomes non-selected by V0 level output from every output of segment drivers and every output of common drivers.</td><td>Controller</td></tr>
<tr><td>CS</td><td>I</td><td>COM / SEG mode control</td><td>When CS = "Low", RA0086A is used as an 80-bit segment driver.
When CS = "High", RA0086A is set to an 80-bit common driver</td><td>VDD/ VSS</td></tr>
<tr><td>AMS</td><td>I</td><td>Application mode select</td><td>According to the input value of the AMS and the CS pin, application mode of RA0086A is differs as shown below.
<table>
<tr><th>CS</th><th>AMS</th><th>Application mode</th><th>COM /SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel interface mode.</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial interface mode.</td></tr>
<tr><td>1</td><td>0</td><td>Single type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual type application mode</td></tr>
</table></td><td>VDD/ VSS</td></tr>
</table>

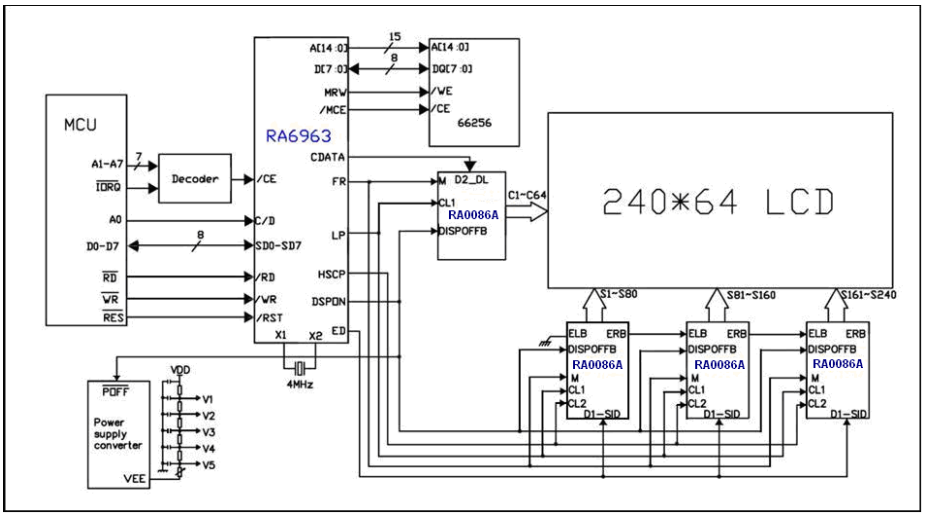
<table>
<tr><td>D1_SID, D2_DL, D3_DM, D4_DR.</td><td>I/O</td><td>Display data input / Serial input data / left,right data input output</td><td>- In segment driver application mode, these pins are used as 4-bit data input pin (when 4-bit parallel interface mode : AMS = "Low"), or D1_SID is used as serial data input pin and other pins are not used (connect these to VDD) (when 1-bit serial interface mode : AMS = "High").

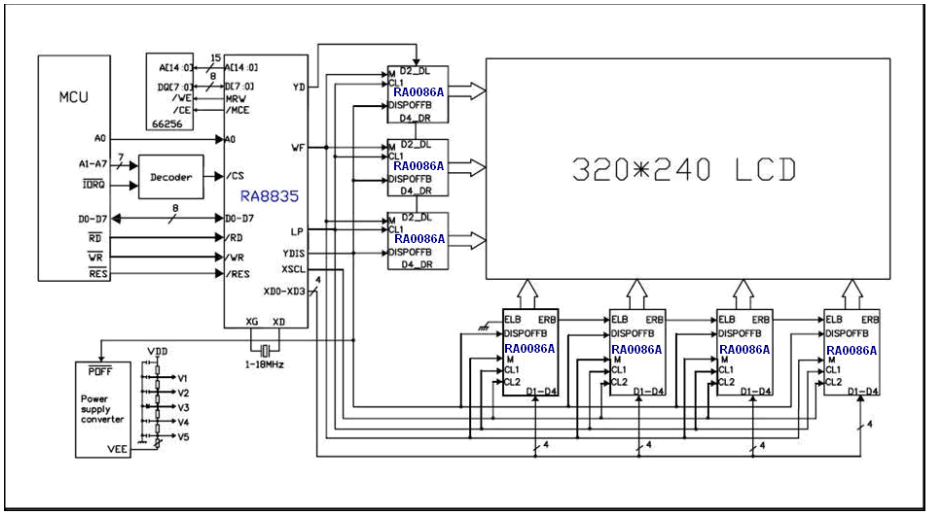
– In common driver application mode, the data is shifted from D2_DL(D4_DR) to D4_DR(D2_DL), when in single type interface mode (AMS = "Low"). In dual type application case, the data are shifted from D2_DL and D3_DM (D4_DR and D3_DM) to D4_DR(D2_DL). In each case the direction of the data shift and the connection of data pins are determined by SHL input.</td><td>Controller</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction control</td><td>When SHL = "Low", data is shifted from left to right.
When SHL = "High", the direction is reversed.</td><td>VDD/ VSS</td></tr>
<tr><td>ELB,ERB</td><td>I/O</td><td>Enable data input/output</td><td>– In segment driver application mode, the internal operation is enabled only when enable input (ELB or ERB) is “Low” (power down function). When several drivers are serially connected, the enable state of each driver is shifted according to the SHL input. Connect these pins as below.
<table>
<tr><td rowspan="2">SHL</td><td colspan="2">Segment Driver</td></tr>
<tr><td>ELB</td><td>ERB</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
</table>
- In common driver application mode, power down function is not used. Open these pins.</td><td></td></tr>
</table>

5. System Block Diagram



6. Application Information





7. Package