

**RAiO**

**RA8808**

**128x64 Driver  
for Dot Matrix LCD**

**Specification**

Version 1.0

March 26, 2009

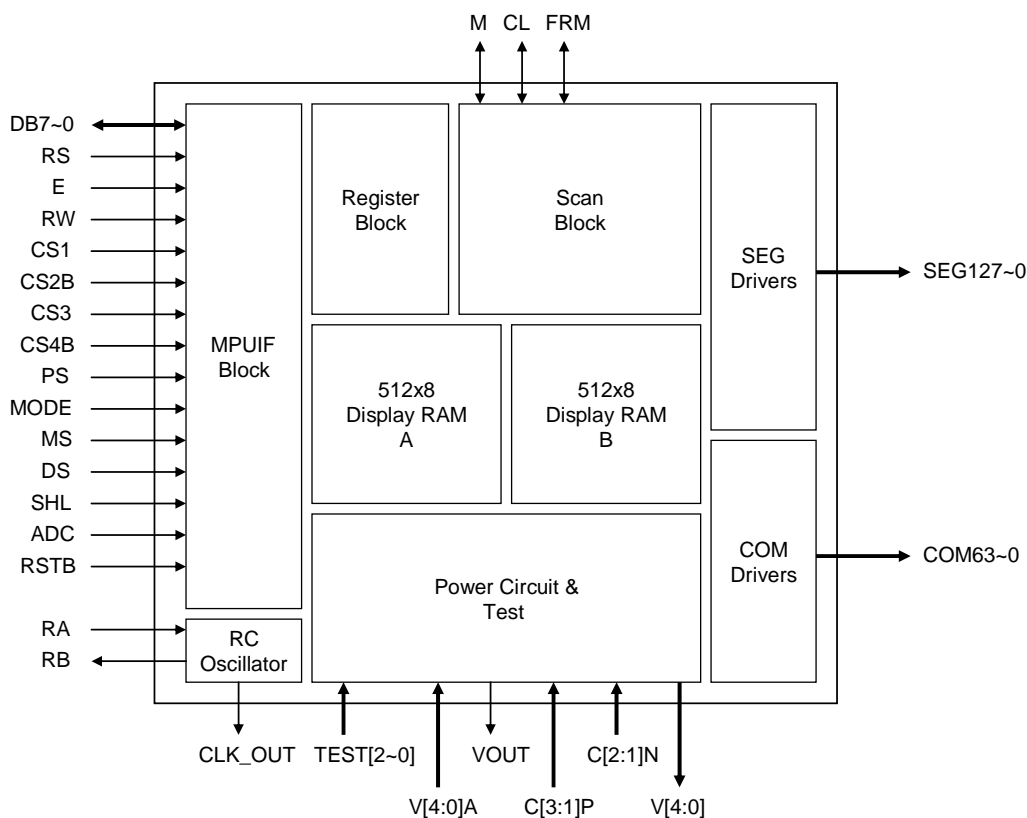
## 1. General Description

The RA8808 is a LCD driver LSI with 128(Segment) x 64(Common) driver output for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 128-bit segment drivers, 64-bit common drivers and decoder logic. It has the internal display RAM for storing the display data transferred from an 8-bit 8080/6800 micro controller or 3-wire-SPI/IIC controller and generates the dot matrix liquid crystal driving signals corresponding to stored data.

## 2. Features

- ◆ Dot matrix LCD segment driver with 128 channel output, and common driver with 64 channel output.
- ◆ Internal timing generator circuit for dynamic display.
- ◆ Selection of master/slave mode for combine two RA8808 controller to support 256x64 dot Matrix.
- ◆ Applicable LCD common duty: 1/48, 1/64.
- ◆ Support 6800/8080 8-bit parallel MPU interface.
- ◆ Support 3-wires SPI and IIC serial MPU interface.
- ◆ Two 512 bytes (4096-bits) Display RAM
- ◆ LCD driving voltage: 8V ~17V
- ◆ Built-in 2X~4X Voltage Booster and Voltage Follower
- ◆ Power supply voltage: +2.7V ~ 5.5V
- ◆ High voltage CMOS process
- ◆ Bare gold bump chip available

## 3. Block Diagram





<p><b>RW</b></p>	<p> </p>	<p><b>In Parallel Mode :</b> Read-Write Control or Write Control When use 6800 series interface, this pin is used as data read/write control. Active high for read and active low for write. When use 8080 series interface, this pin is used as data write, active low.</p> <p><b>In Serial Mode :</b> This pin is not used and must be connected to low.</p>															
<p><b>RS</b></p>	<p> </p>	<p><b>In Parallel Mode :</b> <b>Data or Instruction</b> RS = H → DB0~DB7 : Display RAM data RS = L → DB0~DB7 : Instruction data</p> <p><b>In Serial Mode :</b> This pin is not used and must be connected to low.</p>															
<p><b>CS1 CS2B</b></p>	<p> </p>	<p><b>In Parallel Mode :</b> Chip selection for left side (Note 1) In order to interface left side data for input or output, the terminals have to be CS1 = H, CS2B = L.</p> <p><b>In Serial Mode :</b> These pins are not used and must be connected to high or low.</p>															
<p><b>CS3 CS4B</b></p>	<p> </p>	<p><b>In Parallel Mode :</b> Chip selection for right side (Note 1) In order to interface right side data for input or output, the terminals have to be CS3 = H, CS4B = L.</p> <p><b>In Serial Mode :</b> These pins are not used and must be connected to to high or low.</p>															
<p><b>RSTB</b></p>	<p> </p>	<p><b>Reset Signal</b> When RSTB = L, _ON/OFF register becomes set by 0. (display off) _Display start line register becomes set by 0.(Z-address 0 set, display from line 0) After releasing reset, this condition can be changed only by instruction.</p>															
<p><b>PS</b></p>	<p> </p>	<p><b>Parallel/Serial MPU Interface Selection</b></p> <table border="1" data-bbox="566 1422 1093 1534"> <thead> <tr> <th>PS</th> <th>Parallel/Serial</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Parallel</td> </tr> <tr> <td>L</td> <td>Serial</td> </tr> </tbody> </table>	PS	Parallel/Serial	H	Parallel	L	Serial									
PS	Parallel/Serial																
H	Parallel																
L	Serial																
<p><b>MODE</b></p>	<p> </p>	<p><b>MPU Interface Selection(Combine with PS)</b></p> <table border="1" data-bbox="566 1601 1189 1769"> <thead> <tr> <th>PS</th> <th>MODE</th> <th>MPU Interface</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>6800 series</td> </tr> <tr> <td>H</td> <td>L</td> <td>8080 series</td> </tr> <tr> <td>L</td> <td>H</td> <td>3-wire SPI</td> </tr> <tr> <td>L</td> <td>L</td> <td>IIC</td> </tr> </tbody> </table>	PS	MODE	MPU Interface	H	H	6800 series	H	L	8080 series	L	H	3-wire SPI	L	L	IIC
PS	MODE	MPU Interface															
H	H	6800 series															
H	L	8080 series															
L	H	3-wire SPI															
L	L	IIC															

5-2 LCD Panel Interface

Pin Name	I/O	Description															
SEG0~ SEG127	O	<p><b>LCD Segment Driver Output</b> Display RAM data 1 : On, Display RAM data 0 : Off Relation of display RAM &amp; M :</p> <table border="1"> <thead> <tr> <th>M</th> <th>Data</th> <th>Output Level</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>V2</td> </tr> <tr> <td>L</td> <td>H</td> <td>V0</td> </tr> <tr> <td>H</td> <td>L</td> <td>V3</td> </tr> <tr> <td>H</td> <td>H</td> <td>GND</td> </tr> </tbody> </table>	M	Data	Output Level	L	L	V2	L	H	V0	H	L	V3	H	H	GND
M	Data	Output Level															
L	L	V2															
L	H	V0															
H	L	V3															
H	H	GND															
COM0~ COM63	O	<p><b>Common Signal Output for LCD Driving</b> Relation of common signal &amp; M :</p> <table border="1"> <thead> <tr> <th>M</th> <th>Common Signal</th> <th>Output Level</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>V1</td> </tr> <tr> <td>L</td> <td>H</td> <td>GND</td> </tr> <tr> <td>H</td> <td>L</td> <td>V4</td> </tr> <tr> <td>H</td> <td>H</td> <td>V0</td> </tr> </tbody> </table>	M	Common Signal	Output Level	L	L	V1	L	H	GND	H	L	V4	H	H	V0
M	Common Signal	Output Level															
L	L	V1															
L	H	GND															
H	L	V4															
H	H	V0															
M	I/O	<p><b>Alternating Signal Input for LCD Driving.</b> The input/output selection is determined by MS.</p>															
CL	I/O	<p><b>Display Synchronous Signal</b> Display data is latched at rising time of the CL signal and increments the Z-address counter at CL falling time. The input/output selection is determined by MS.</p>															
FRM	I/O	<p><b>Synchronous Control Signal</b> Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high. The input/output selection is determined by MS.</p>															
MS	I	<p><b>Master/Slave Mode Selection</b></p> <table border="1"> <thead> <tr> <th>MS</th> <th>Master/Slave Mode</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Master</td> </tr> <tr> <td>L</td> <td>Slave</td> </tr> </tbody> </table> <p>When in Master mode, M, CL, FRM are output pins. When in Slave mode, M, CL, FRM are input pins.</p>	MS	Master/Slave Mode	H	Master	L	Slave									
MS	Master/Slave Mode																
H	Master																
L	Slave																

5-3 Clock

Pin Name	I/O	Description				
RA	I	<p>In internal clock mode, this pin connects to external resistor for RC circuit. In external clock mode, this pin is an input of external clock.</p> <table border="1"> <thead> <tr> <th>Internal Clock Mode</th> <th>External Clock Mode</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> </tr> </tbody> </table>	Internal Clock Mode	External Clock Mode		
Internal Clock Mode	External Clock Mode					
RB	O	<p>In internal clock mode, this pin connects to external resistor for RC circuit. In external clock mode, this pin must keep floating.</p>				
CLK_OUT	O	<p>Internal system clock output for cascade application or others for user.</p>				

**5-4 Power**

Pin Name	I/O	Description
VOUT	O	Regulator Voltage Output
VDD VDDP	P	Digital Power
GND GNDP	P	Digital Ground
AVDD	P	Analog Power
AGND	P	Analog Ground
C1N C1P	I	<b>Capacitor Input</b> These are used to connect a capacitor for internal Booster.
C2N C2P	I	<b>Capacitor Input</b> These are used to connect a capacitor for internal Booster.
C3P	I	<b>Capacitor Input</b> These are used to connect a capacitor for internal Booster.
V0A~V4A	I	<b>Voltage Input</b>
V0~V4	O	<b>Voltage Source of LCD Driver</b> The relationship of the power is V0 > V1 > V2 > V3 > V4 > GND.

**5-5 MISC**

Pin Name	I/O	Description						
ADC	I	<b>Selection of Segment Data Direction</b> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>ADC</th> <th>Common Data Shift Direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>SEG0 → SEG1 ... → SEG127</td> </tr> <tr> <td>L</td> <td>SEG127 → SEG126 ... → SEG0</td> </tr> </tbody> </table>	ADC	Common Data Shift Direction	H	SEG0 → SEG1 ... → SEG127	L	SEG127 → SEG126 ... → SEG0
ADC	Common Data Shift Direction							
H	SEG0 → SEG1 ... → SEG127							
L	SEG127 → SEG126 ... → SEG0							
SHL	I	<b>Selection of Common Data Shift Direction</b> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>Common Data Shift Direction</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>COM0 → COM1 ... → COM63</td> </tr> <tr> <td>L</td> <td>COM63 → COM62 ... → COM0</td> </tr> </tbody> </table>	SHL	Common Data Shift Direction	H	COM0 → COM1 ... → COM63	L	COM63 → COM62 ... → COM0
SHL	Common Data Shift Direction							
H	COM0 → COM1 ... → COM63							
L	COM63 → COM62 ... → COM0							
DS	I	<b>Selection of Display Duty</b> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DS</th> <th>Duty</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>1/64</td> </tr> <tr> <td>L</td> <td>1/48</td> </tr> </tbody> </table>	DS	Duty	H	1/64	L	1/48
DS	Duty							
H	1/64							
L	1/48							
TEST0 TEST1 TEST2	I	These pins must contact to GND in normal mode.						

**6. LCD Panel Interface Application Circuit**

